Fig.1(a) (Prior Art)

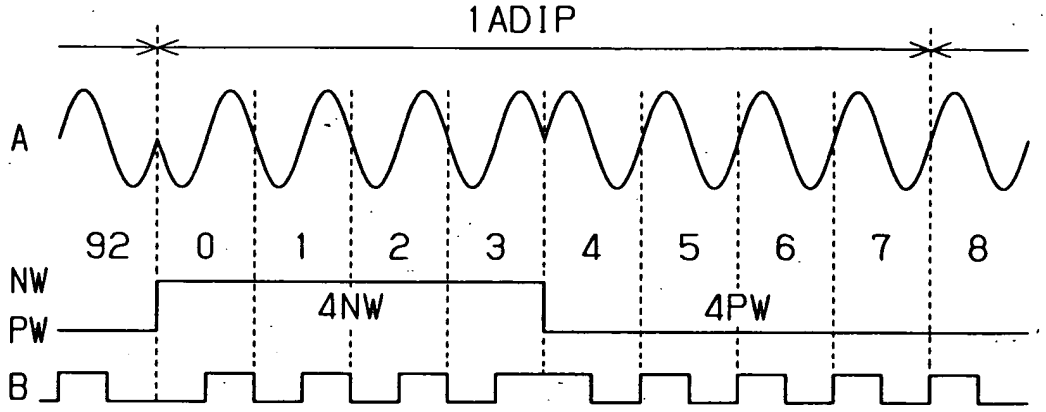


Fig.1(b) (Prior Art)

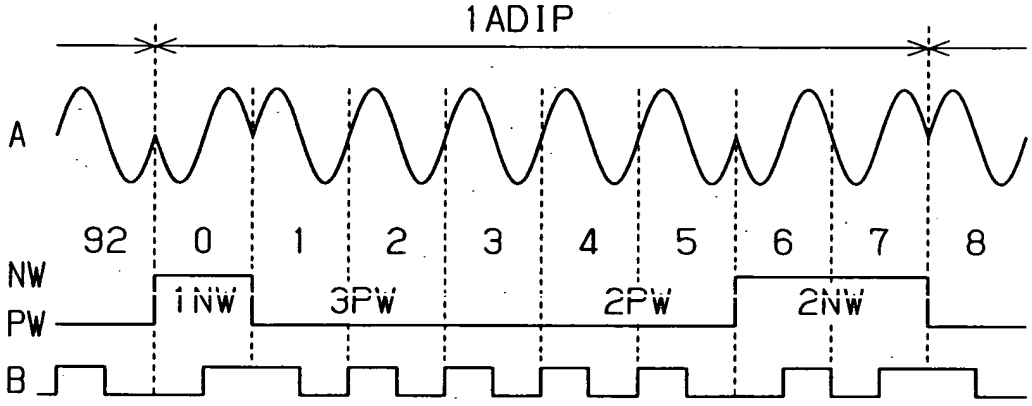


Fig.1(c) (Prior Art)

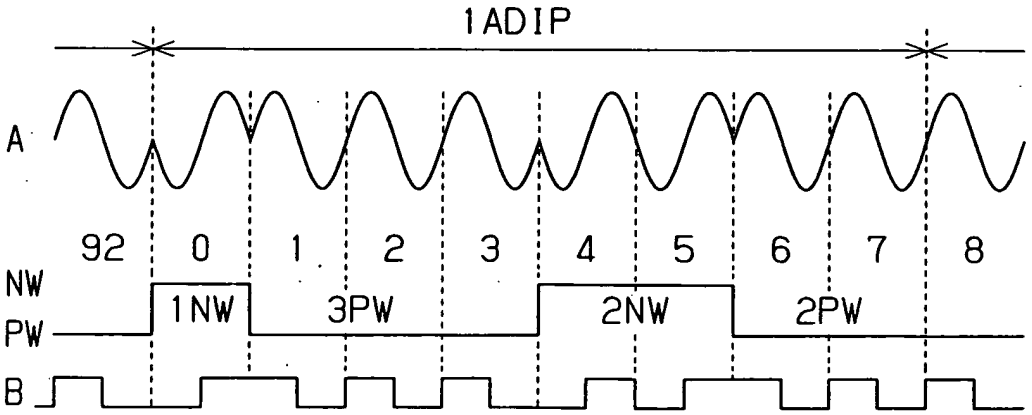


Fig.2

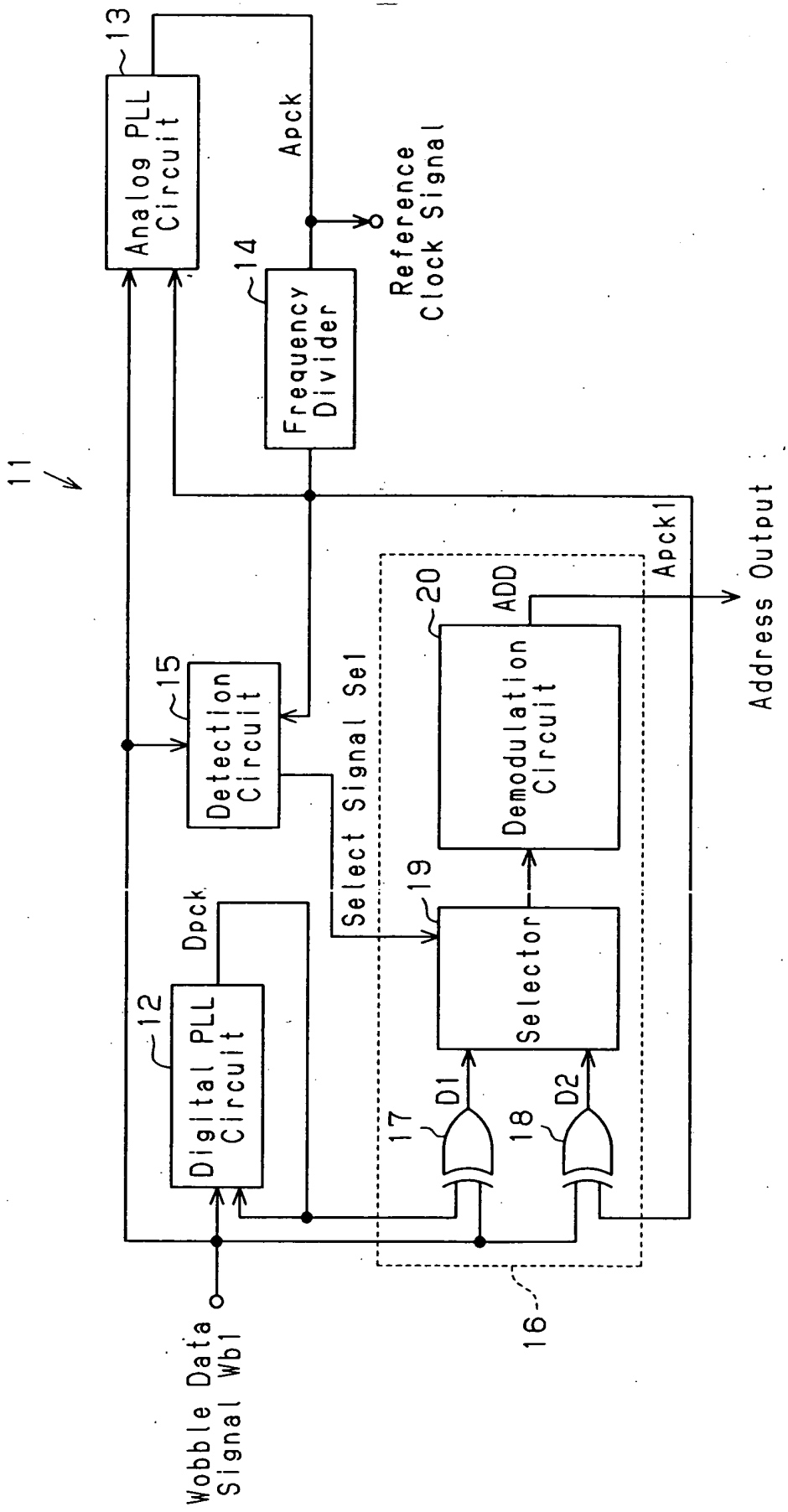

11
13
Analog PLL Circuit
Apck
Reference Clock Signal
14
Frequency Divider
15
Detection Circuit
Select Signal Sel
20
ADD
Demodulation Circuit
Apck1
Address Output
19
Selector
Dpck
12
Digital PLL Circuit
17
D1
18
D2
16
Wobble Data Signal Wb1

Fig.3

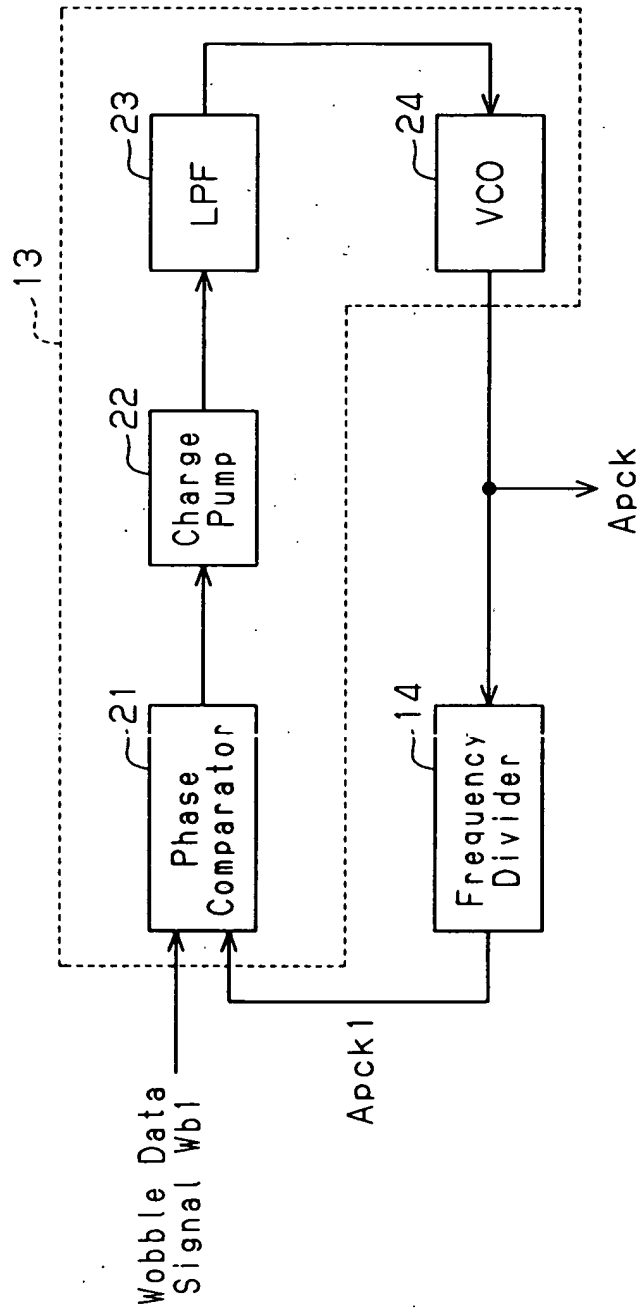
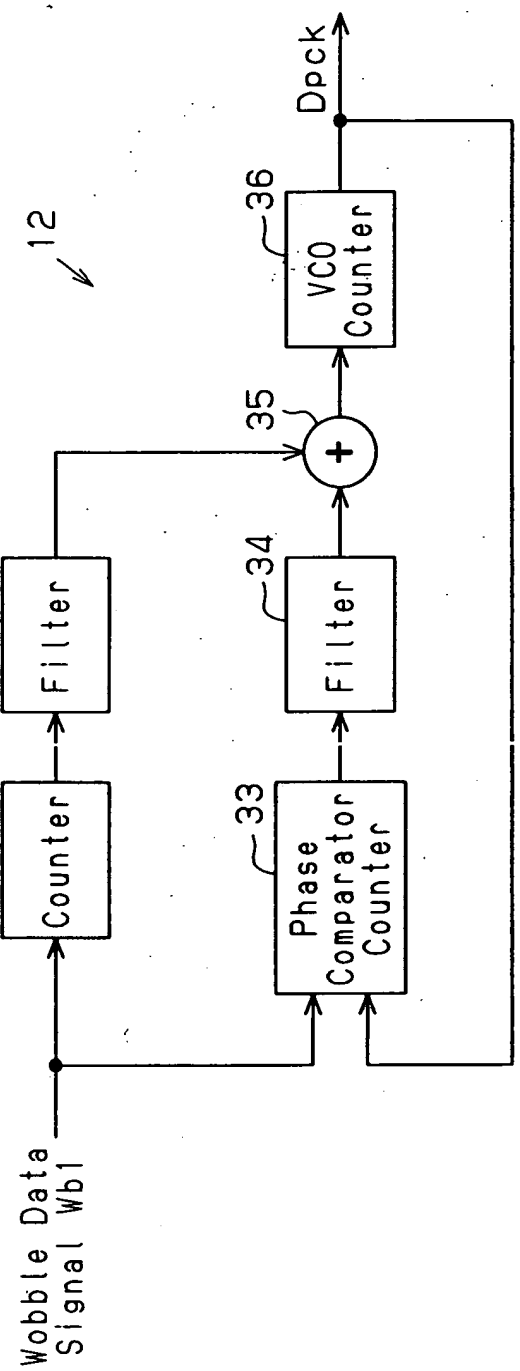

13
23
LPF
24
VCO
22
Charge Pump
21
Phase Comparator
14
Frequency Divider
Apck
Apck1
Wobble Data Signal Wb1

Fig.4


12
Dpck
36
VCO Counter
35
+
32
Filter
34
Filter
31
Counter
33
Phase Comparator Counter
Wobble Data Signal Wb1